User's Guide

NHD-19232WG-BGGH-V#T

LCM

(Liquid Crystal Display Graphic Module)

RoHS Compliant

NHD-	Newhaven Display
19232-	192 x 32 pixels
WG-	W= Factory Line G= Display Type: Graphic
B-	Model/Serial Number
G-	Green LED B/L
G-	STN- Gray
H-	Transflectine, 6:00 View, Wide Temperature (-20 ~ +70c)
V#T-	With Built-in Positive Voltage Supply; RoHS

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February 29, 2008

Contents

1. Module Classification Information

NHD 19232 W G - B G G H - **V#** T

① ② ③ ④ ⑤ ⑥ ⑦ ⑧ 9

① Brand：Newhaven Display

② Display Font：192 x 32 Dots

③ Factory Line: W

④ Display Type：H→ Character Type, G→ Graphic Type, C→ Color

⑤ Model / Serial number: **B**

⑥ Backlight Type：

N→ Without backlight
B→ EL, Blue green
D→ EL, Green
W→ EL, White
F→ CCFL, White
Y→ LED, Yellow Green
T→ LED, White
A→ LED, Amber
R→ LED, Red
O→ LED, Orange
G→ LED, Green
P→ LED, Blue

⑦ LCD Mode：

B→ TN Positive, Gray
T→ FSTN Negative
N→ TN Negative,
G→ STN Positive, Gray
Y→ STN Positive, Yellow Green
M→ STN Negative, Blue
F→ FSTN Positive

⑧ LCD Polarize Type/ Temperature range/ View direction

A→ Reflective, N.T, 6:00
D→ Reflective, N.T, 12:00
G→ Reflective, W. T, 6:00
J→ Reflective, W. T, 12:00
B→ Transflective, N.T,6:00
E→ Transflective, N.T.12:00
H→ Transflective, W.T,6:00
K→ Transflective, W.T,12:00
C→ Transmissive, N.T,6:00
F→ Transmissive, N.T,12:00
I→ Transmissive, W. T, 6:00
L→ Transmissive, W.T,12:00

9 Special Code

V : Built-in Positive Voltage
#T: RoHS

2. Precautions in use of LCD Modules

(1) Avoid applying excessive shock to the module or making any alterations or modifications to it.
(2) Don't make extra holes on the printed circuit board, modify its shape or change the components of LCD module.
(3) Don't disassemble the LCM.
(4) Don't operate it above the absolute maximum rating.
(5) Don't drop, bend or twist LCM.
(6) Soldering: only to the I/O terminals.
(7) Storage: please store in anti-static electricity container and clean environment.

3. General Specification for : NHD-19232WG-BGGH-V#T

Item	Dimension	Unit
Number of Characters	192 x 32 dot	-
Module dimension	116.0 x 37.0 x 13.9(MAX)	mm
View area	84.0 x 18.6	mm
Active area	80.6 x 15.96	mm
Dot size	0.46 x 0.38	mm
Dot pitch	0.5 x 0.42	mm
LCD type	STN-**G**ray, Positive, Transflective	
Duty	1/32	
View direction	6 o'clock	
Backlight Type	LED Green	

4. Absolute Maximum Ratings

Item	Symbol	Min	Typ	Max	Unit
Operating Temperature	T_{OP}	-20	-	+70	℃
Storage Temperature	T_{ST}	-30	-	+80	℃
Input Voltage	V_I	0	-	V_{DD}	V
Supply Voltage For Logic	V_{DD}	0	-	6.7	V
Supply Voltage For LCD	V_O-V_{SS}	0	-	7.0	V

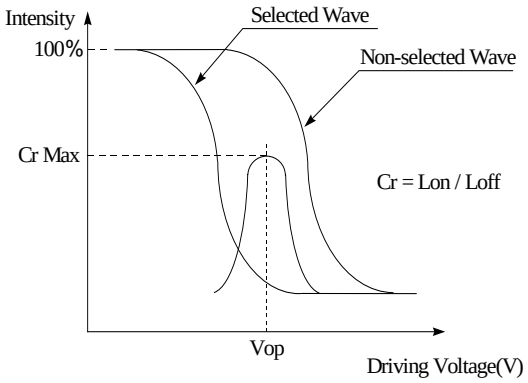
5. Electrical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage For Logic	V_{DD}-V_{SS}	-	4.5	5.0	5.5	V
Supply Voltage For LCD	V_O-V_{SS}	Ta=-20℃ Ta=25℃ Ta=+70℃	- - 3.8	- 4.5 -	5.5 - -	V V V
Input High Volt.	V_{IH}	-	0.7V_{DD}	-	V_{DD}	V
Input Low Volt.	V_{IL}	-	0	-	0.3V_{DD}	V
Output High Volt.	V_{OH}	-	2.4	-	-	V
Output Low Volt.	V_{OL}	-	-	-	0.4	V
Supply Current	I_{DD}	-	-	2.6	3	mA

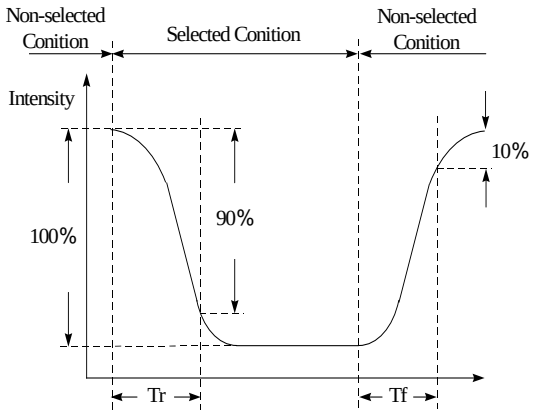
6. Optical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
View Angle	(V)θ	CR≧ 2	20	-	40	deg
	(H)φ	CR≧ 2	-30	-	30	deg
Contrast Ratio	CR	-	-	3	-	-
Response Time	T rise	-	-	200	300	ms
	T fall	-	-	200	300	ms

Definition of Operation Voltage (Vop) **Definition of Response Time (Tr , Tf)**



[positive type]



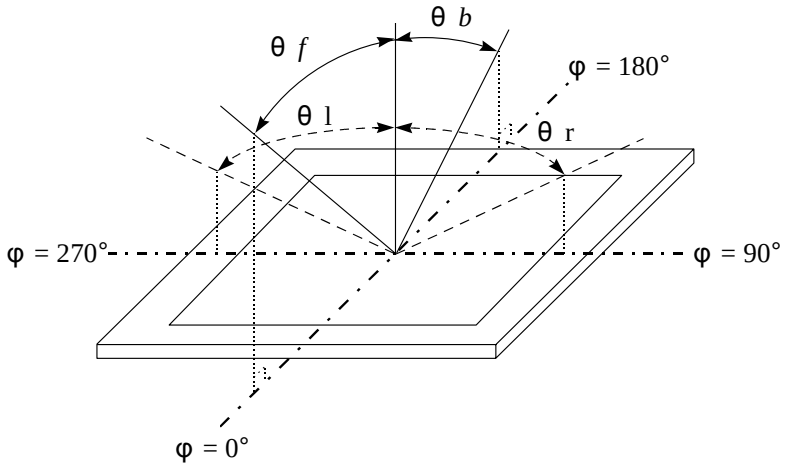
[positive type]

Conditions:

Operating Voltage : Vop Viewing Angle (θ , φ) : 0° , 0°

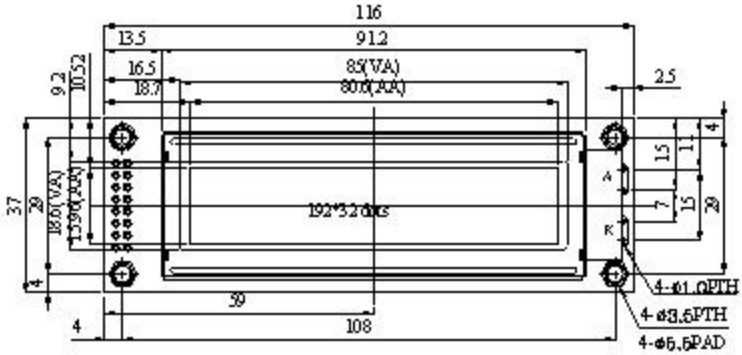
Frame Frequency : 64 HZ Driving Waveform : 1/N duty , 1/a bias

Definition of viewing angle (CR≧ 2)

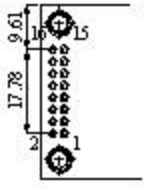


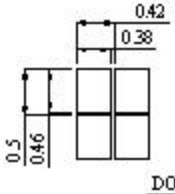
7. Interface Description

Pin No.	Symbol	Level	Description
1	**VSS**	**0V**	**Ground**
2	**VDD**	**5.0V**	**Supply voltage for logic**
3	**V_O**		**Supply voltage for LCD**
4	**RS**		**H: Data, L : Instruction**
5	**R/W**	**H/L**	**H: Read (MPU← Module) , L: Write (MPU→ Module)**
6	**E**	**H/L**	**ENABLE SIGNAL**
7	**DB0**	**H/L**	**Data bus**
8	**DB1**	**H/L**	**Data bus**
9	**DB2**	**H/L**	**Data bus**
10	**DB3**	**H/L**	**Data bus**
11	**DB4**	**H/L**	**Data bus**
12	**DB5**	**H/L**	**Data bus**
13	**DB6**	**H/L**	**Data bus**
14	**DB7**	**H/L**	**Data bus**
15	**A/VEE**	**-**	**Positive Voltage Output**
16	**K**	**-**	**NC**

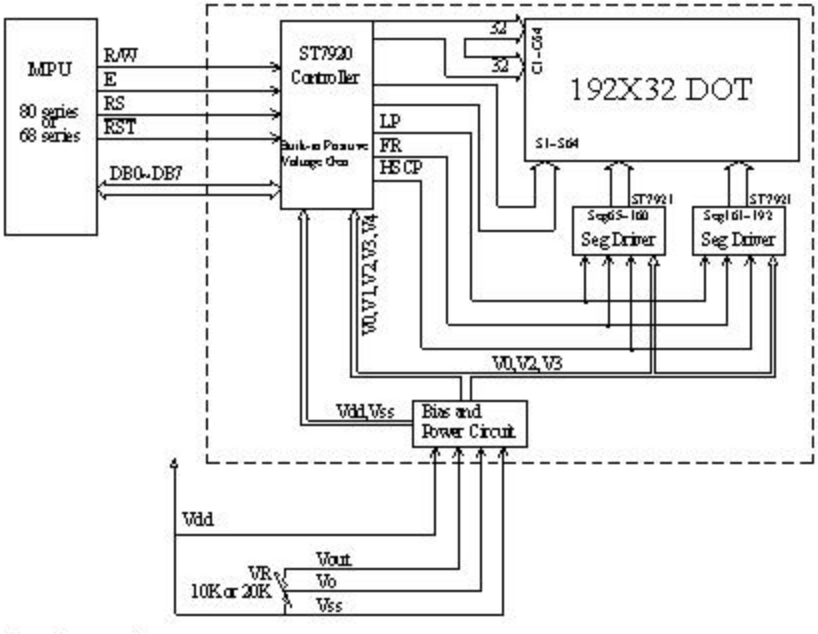


PIN NO.	SYMBOL
1	Vss
2	Vdd
3	VO
4	RS
5	R/$\overline{W}$
6	E
7	DB0
8	DB1
9	DB2
10	DB3
11	DB4
12	DB5
13	DB6
14	DB7
15	A
16	K





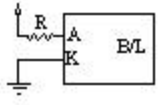
DOT Size
Scale 20/1



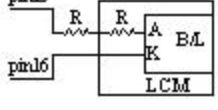
External contrast adjustment.

LED B/L Drive Method

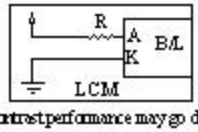
1.Drive from A,K



2.Drive from pin15, pin16



3.Drive from Vdd,Vss



(Contrast performance may go down.)

9. Function Description

Function Description：

System interface

ST7920 supports 3 kinds of bus interface to MPU. 8 bits parallel, 4 bits parallel and clock synchronized serial interface. Parallel interface is selected by PSB="I" and serial interface by PSB="0". 8 bit / 4 bit interface is selected by function set instruction DL bit.

Two 8 bit registers (data register DR, instruction register IR) are used in ST7920's write and read operation. Data Register (DR) can access DDRAM/CGRAM/GDRAM and IRAM's data through the address pointer implemented by Address Counter (AC). Instruction Register (IR) stores the instruction by MPU to ST7920.

4 modes of read/write operation specified by RS and RW：

RS	RW	Description
L	L	MPU write instruction to instruction register (IR)
L	H	MPU read busy flag (BF) and address counter (AC)
H	L	MPU write data to data register (DR)
H	H	MPU read data from data register (DR)

Busy Flag (BF)

Internal operation is in progress when BF="I", ST7920 is in busy state. No new instruction will be accepted until BF="0". MPU must check BF to determine whether the internal operation is finished and new instruction can be sent.

Address counter (AC)

Address counter (AC)is used for address pointer of DDRAM/CGRAM/IRAM/GDRAM. (AC) can be set by instruction and after data read or write to the memories (AC) will increase or decrease by 1 according to the setting in "entry mode set". When RS="0" and RW= "1" and E="1" the value of (AC) will output to DB6~DB0.

16x16 character generation ROM (CGROM) and 8x16 half height ROM (HCGROM)

ST7920 provides character generation ROM supporting 8192 16 x 16 character fonts and 126 8 x 16 alphanumeric characters. It is easy to support multi languages application such as Chinese and English. Two consecutive bytes are used to specify one 16x16 character or two 8x16 half-height characters. Character codes are written into DDRAM and the corresponding fonts are mapped from CGROM or HCGROM to the display drivers.

Character generation RAM (CGRAM)

ST7920 provides RAM to support user-defined fonts. Four sets of 16x16 bit map area are available. These user-defined fonts are displayed the same ways as CGROM fonts through writing character cod data to DDRAM

ICON RAM (IRAM)

ST7920 provides 240 ICON display. It consists of 15 sets of IRAM address. Each IRAM address has 16 bits data IRAM address should be set first before writing to the IRAM. Two bytes for each address. First higher byte (D15~D8) and then lower byte (D7~D0).

Display data RAM (DDRAM)

There are 64x2 bytes for display data RAM area. Can store display data for 16 characters (16x16) by 4 lines or 32 characters (8x16) by 4 lines. However, only 2 lines can be displayed at a time. Character codes stored in DDRAM point to the fonts specified by CGROM, HCGROM and CGRAM. ST7920 display half height HCGROM fonts, user-defined CGRAM fonts and full 16x16 CGROM fonts. Data codes 0000H~0006H are for CGRAM user-defined fonts. Data codes 02H~7FH are for half height alphanumeric fonts. Data codes (A140--~D75F) are for BIG5 code and (A1A0~F7FF) are for GB code.

1. Display HCGROM fonts: Write 2 bytes data to DDRAM to display two 8x16 fonts. Each byte represents 1 character font. The data of each byte is 02H~7FH.

2. Display CGRAM fonts: Write 2 bytes data to DDRAM to display one 16x16 font. Only 0000H, 0002H, 0004H, 0006H are allowed.

3. Display CGROM fonts: Write 2 bytes data to DDRAM to display one 16x16 font. A140H~D75FH are for (BIG5) code, A1A0H~F7FFH are for (GB) code.

Higher byte (D15--, D8) are written first and then lower byte (D7~DO) . Refer to Table 5 for address map

CGRAM fonts and CGROM fonts can only be displayed in the start position of each address. (Refer to Table 4)

80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F
H L	H L	H L	H L	H L	H L	H L	H L	H L	H L	H L	H L	H L	H L	H L	H L
S I	t r	o n	I x		S	T 7	9 2	0							
矽	創	電	子	·	中	文	編	碼	(	正	確	)			
矽	創	電	子			中	文	編	碼						

Table 4

Incorrect position

Graphic RAM (GDRAM)

Graphic display RAM supports 64x256 bits bit-mapped memory space. GDRAM address is set by writing 2 consecutive bytes for vertical address and horizontal address. Two-bytes data write to GDRAM for one address. Address counter will automatically increase by one for the next two-byte data. The procedure is as followings.

1. Set vertical address (Y) for GDRAM

2. Set horizontal address (X) for GDRAM

3. Write D 15~ D8 to GDRAM (first byte)

4. Write D7~D0 to GDRAM (second byte)

Graphic display memory map please refer to Table-8

LCD driver

LCD driver have 33 common and 64 segments to drive the LCD panel. Segment data from CGRAM /CGROM/HCGROM are shifted into the 64 bits segment latches to display. Extended segment driver ST7921 can be used to extend the segment drivers to 256.

DDRAM data (char. code)					CGRAM Addr.						CGRAM data (higher byte)								CGRAM data (lower byte)							
B15~ B4	B3	B2	B1	B0	B5	B4	B3	B2	B1	B0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	X	00	X	00	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	0	0	0	0	0
							0	0	0	1	1	1	1	1	1	1	1	0	0	1	0	0	0	0	0	0
							0	0	1	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	0
							0	0	1	1	0	0	0	1	0	0	0	0	0	1	1	1	1	1	1	0
							0	1	0	0	0	0	1	0	0	1	0	0	1	0	0	0	0	1	0	0
							0	1	0	1	0	0	1	1	1	1	0	0	1	0	0	0	0	1	0	0
							0	1	1	0	0	1	1	0	0	1	0	1	0	1	0	0	1	0	0	0
							0	1	1	1	1	0	1	0	0	1	1	0	0	1	0	0	1	0	0	0
							1	0	0	0	0	0	1	0	0	1	0	0	0	1	0	1	0	0	0	0
							1	0	0	1	0	0	1	0	0	1	0	0	0	0	0	1	0	0	0	0
							1	0	1	0	0	0	1	0	0	1	0	0	0	0	0	1	0	0	0	0
							1	0	1	1	0	0	1	1	1	1	0	0	0	0	0	1	0	0	0	0
							1	1	0	0	0	0	1	0	0	1	0	0	0	1	0	0	0	0	0	0
							1	1	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
							1	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
							1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	X	01	X	01	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	1	1	0
							0	0	0	1	0	0	0	0	1	1	0	1	0	0	0	0	0	0	1	0
							0	0	1	0	0	0	1	0	0	0	0	1	0	0	1	1	0	1	0	0
							0	0	1	1	0	1	0	1	1	1	0	1	1	0	1	0	0	1	0	0
							0	1	0	0	1	0	0	0	0	0	0	1	0	0	1	0	0	1	0	0
							0	1	0	1	0	1	1	1	1	1	1	1	0	0	1	0	0	1	0	0
							0	1	1	0	0	1	0	0	0	0	0	1	0	0	1	0	0	1	0	0
							0	1	1	1	0	1	0	0	0	0	0	1	0	0	1	0	0	1	0	0
							1	0	0	0	0	1	0	0	0	0	0	1	0	0	1	0	0	1	0	0
							1	0	0	1	0	1	1	1	1	1	1	1	0	0	1	0	0	1	0	0
							1	0	1	0	0	1	0	0	0	0	0	1	0	0	1	0	0	1	0	0
							1	0	1	1	0	1	1	1	1	1	1	1	0	0	1	0	0	1	0	0
							1	1	0	0	1	0	1	0	0	0	0	1	0	1	0	0	1	0	0	0
							1	1	0	1	1	0	1	1	1	1	1	1	0	0	1	1	1	0	0	0
							1	1	1	0	1	0	1	0	0	0	0	1	0	0	0	1	0	0	0	0
							1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5：**DDRAM data（character code），CGRAM data / address map**

Note

1. DDRAM data (character code) bit1 and bit2 are the same as CGRAM address bit4 and bit5.
2. CGRAM address bit0 to bit3 specify total 16 rows. Row16 is for cursor display. The data in row 16 will be logical OR to the cursor.
3. CGRAM data for each address is 16 bits.
4. DDRAM data to select CGRAM bit4 to bit15 must be “0”. Bit0 and bit3 value are “don’t care”.

ICON RAM address Set SR ”0”,and then set IRAM address AC3…AC0				ICON RAM data														
				Higher byte							Lower byte							
AC3	AC2	AC1	AC0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8	SEG9	SEG10	SEG11	SEG12	SEG13	SEG14	SEG15
0	0	0	1	SEG16	SEG17	SEG18	SEG19	SEG20	SEG21	SEG22	SEG23	SEG24	SEG25	SEG26	SEG27	SEG28	SEG29	SEG30	SEG31
0	0	1	0	SEG32	SEG33	SEG34	SEG35	SEG36	SEG37	SEG38	SEG39	SEG40	SEG41	SEG42	SEG43	SEG44	SEG45	SEG46	SEG47
0	0	1	1	SEG48	SEG49	SEG50	SEG51	SEG52	SEG53	SEG54	SEG55	SEG56	SEG57	SEG58	SEG59	SEG60	SEG61	SEG62	SEG63
0	1	0	0	SEG64	SEG65	SEG66	SEG67	SEG68	SEG69	SEG70	SEG71	SEG72	SEG73	SEG74	SEG75	SEG76	SEG77	SEG78	SEG79
0	1	0	1	SEG80	SEG81	SEG82	SEG83	SEG84	SEG85	SEG86	SEG87	SEG88	SEG89	SEG90	SEG91	SEG92	SEG93	SEG94	SEG95
0	1	1	0	SEG96	SEG97	SEG98	SEG99	SEG100	SEG101	SEG102	SEG103	SEG104	SEG105	SEG106	SEG107	SEG108	SEG109	SEG110	SEG111
0	1	1	1	SEG112	SEG113	SEG114	SEG115	SEG116	SEG117	SEG118	SEG119	SEG120	SEG121	SEG122	SEG123	SEG124	SEG125	SEG126	SEG127
1	0	0	0	SEG128	SEG129	SEG130	SEG131	SEG132	SEG133	SEG134	SEG135	SEG136	SEG137	SEG138	SEG139	SEG140	SEG141	SEG142	SEG143
1	0	0	1	SEG144	SEG145	SEG146	SEG147	SEG148	SEG149	SEG150	SEG151	SEG152	SEG153	SEG154	SEG155	SEG156	SEG157	SEG158	SEG159
1	0	1	0	SEG160	SEG161	SEG162	SEG163	SEG164	SEG165	SEG166	SEG167	SEG168	SEG169	SEG170	SEG171	SEG172	SEG173	SEG174	SEG175
1	0	1	1	SEG176	SEG177	SEG178	SEG179	SEG180	SEG181	SEG182	SEG183	SEG184	SEG185	SEG186	SEG187	SEG188	SEG189	SEG190	SEG191
1	1	0	0	SEG192	SEG193	SEG194	SEG195	SEG196	SEG197	SEG198	SEG199	SEG200	SEG201	SEG202	SEG203	SEG204	SEG205	SEG206	SEG207
1	1	0	1	SEG208	SEG209	SEG210	SEG211	SEG212	SEG213	SEG214	SEG215	SEG216	SEG217	SEG218	SEG219	SEG220	SEG221	SEG222	SEG223
1	1	1	0	SEG224	SEG225	SEG226	SEG227	SEG228	SEG229	SEG230	SEG231	SEG232	SEG233	SEG234	SEG235	SEG236	SEG237	SEG238	SEG239
1	1	1	1	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---

Table 6 ICON RAM address, data and segment pins

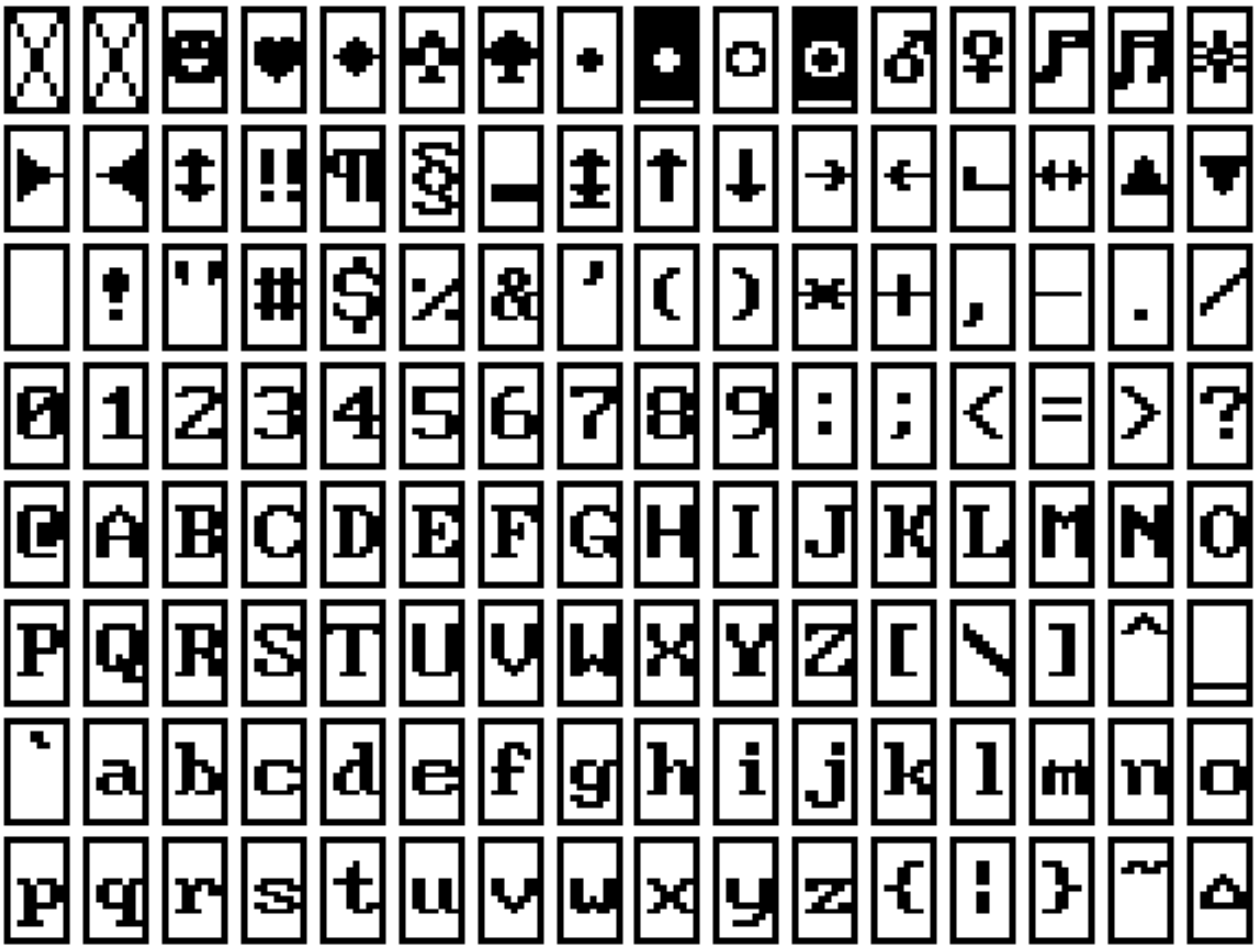


Table 6 16x8 half-height characters

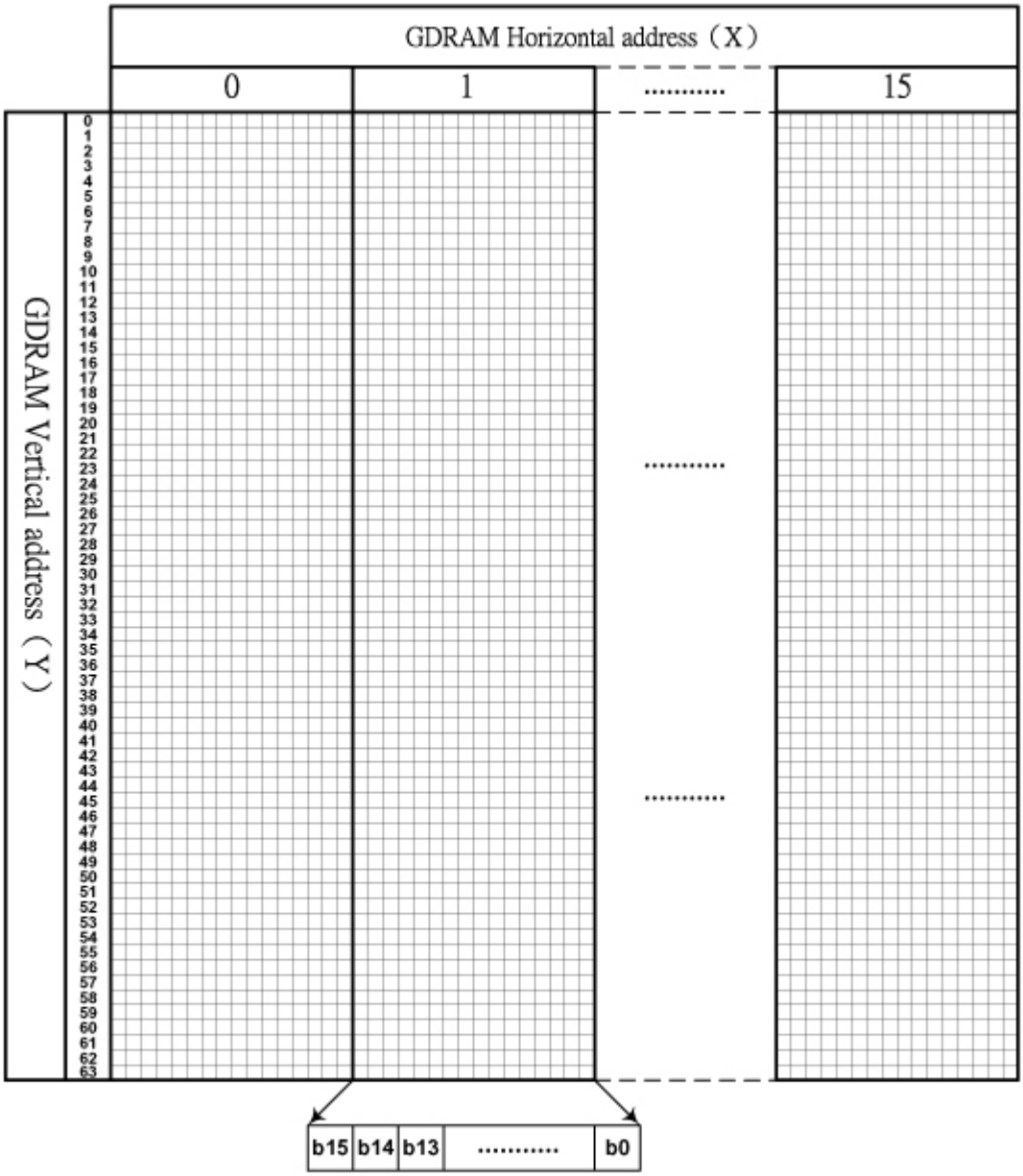


Table 8 GDRAM display coordinates and corresponding address

10. Instructions

Instructions

ST7920 offers basic instruction set and extended instruction set:

Ins	code										Description	Exec time (540KHZ)
	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
CLEAR	0	0	0	0	0	0	0	0	0	1	Fill DDRAM with "20H", and set DDRAM address counter (AC) to "00H"	1.6 ms
HOME	0	0	0	0	0	0	0	0	1	X	Set DDRAM address counter (AC) to "00H", and put cursor to origin; to content of DDRAM are not changed.	72 us
ENTRY MODE	0	0	0	0	0	0	0	1	I/D	S	Set cursor position and shift when doing write or read operation.	72 us
DISPLAY ON/OFF	0	0	0	0	0	0	1	D	C	B	D=1：display ON C=1：cursor ON B=1：blink ON	72 us
CURSOR DISPLAY CONTROL	0	0	0	0	0	1	S/C	R/L	X	X	Cursor position and display shift control； the content of DDRAM are not changed.	72 us
FUNCTION SET	0	0	0	0	1	DL	X	0 RE	X	X	DL=1 8-BIT interface DL=0 4-BIT interface **RE=1：extended instruction** **RE=0：basic instruction**	72 us
SET CGRAM ADDR.	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address to address counter (AC) **Make sure that in extended instruction SR=0 (scroll or RAM address select)**	72 us
SET DDRAM ADDR.	0	0	1	0 AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address to address counter(AC) AC6 is fixed to 0	72 us
READ BUSY FLAG(BF) & ADDR.	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Read busy flag (BF) for completion of internal operation, also Read out the value of address counter(AC)	0 us
WRITE RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data to internal RAM (DDRAM/CGRAM/IRAM/GDRAM)	72 us
READ RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM/IRAM/GDRAM)	72 us

Instruction set 2：(RE=1： extended instruction)

Ins	code										Description	Exec time (540KHZ)
	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
STAND BY	0	0	0	0	0	0	0	0	0	1	Enter stand by mode, any other instruction can terminate (Com1..32 halted, only Com33 ICON can display)	72 us
SCROLL or RAM ADDR. SELECT	0	0	0	0	0	0	0	0	1	SR	SR=1：enable vertical scroll position SR=0：enable IRAM address **(extended instruction)** SR=0：enable CGRAM address **(basic instruction)**	72 us
REVERSE	0	0	0	0	0	0	0	1	R1	R0	Select 1 out of 4 line (in DDRAM) and decide whether to reverse the display by toggling this instruction. **R1, R0 initial value is 00**	72 us
SLEEP	0	0	0	0	0	0	1	SL	X	X	SL=1： leave sleep mode SL=0： enter sleep mode	72 us
EXTENDED FUNCTION SET	0	0	0	0	1	DL	X	1 RE	G	0	DL=1 8-BIT interface DL=0 4-BIT interface **RE=1：extended instruction** **RE=0：basic instruction** G=1： graphic display ON G=0： graphic display OFF	72 us
SET IRAM or SCROLL ADDR	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	SR=1： AC5~AC0 the address of vertical scroll SR=0：AC3~AC0 the address of ICON RAM	72 us
SET GRAPHIC RAM ADDR.	0	0	1	0 AC6	0 AC5	0 AC4	AC3 AC3	AC2 AC2	AC1 AC1	AC0 AC0	Set CGRAM address to address counter (AC) First set vertical address and the horizontal address by consecutive writing. Vertical address range AC6..AC0 Horizontal address range AC3..AC0	72 us

Note：

1. Make sure that ST7920 is not in busy state by reading the busy flag before sending instruction or data. If use delay loop instead please make sure the delay time is enough. Please refer to the instruction execution time.

2. "RE" is the selection bit of basic and extended instruction set. Each time when altering the value of RE it will remain. There is no need to set RE every time when using the same group of instruction set.

Initial setting (Register flag) (RE=0: basic instruction)

Ins	code										Description
	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
ENTRY MODE SET	0	0	0	0	0	0	0	1	I/D	S	Cursor move to right, DDRAM address counter (AC) plus 1
									1	**0**	
DISPLAY STATUS	0	0	0	0	0	0	1	D	C	B	Display, cursor and blink ALL OFF
								0	**0**	**0**	
CURSOR DISPLAY SHIFT	0	0	0	0	0	1	S/C	R/L	X	X	No cursor or display shift operation
							X	**X**			
FUNCTION SET	0	0	0	0	1	DL	X	0 RE	X	X	**8 BIT** MPU interfce, basic instruction set
						1		**0**			

Initial setting (Register flag) (RE=1：extended instruction set)

Ins	code										Description
	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
SCROLL OR RAM ADDR. SELECT	0	0	0	0	0	0	0	1	1	SR	Allow IRAM address or set CGRAM address
										0	
REVERSE	0	0	0	0	0	0	0	1	R1	R0	Begin with normal and toggle to reverse
									0	**0**	
SLEEP	0	0	0	0	0	0	1	SL	X	X	Not in sleep mode
								1			
EXTENDED FUNCTION SET	0	0	0	0	1	DL	X	0 RE	G	X	Graphic display OFF
									0		

Description of basic instruction set

- **CLEAR**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
code	0	0	0	0	0	0	0	0	0	1

Fill DDRAM with "20H"(space code). And set DDRAM address counter (AC to"00H". Set entry mode I/D bit to be "1".

Cursor moves right and AC adds 1 after write or read operation.

- **HOME**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
code	0	0	0	0	0	0	0	0	1	X

Set DDRAM address counter AC to "00H". Cursor moves to origin. Then content of DDRAM is not changed.

- **ENTRY MODE SET**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
code	0	0	0	0	0	0	0	0	1	I/D	S

Set the cursor movement and display shift direction when doing write or read operation.

I/D :address counter increase / decrease

When I/D = "1", cursor moves right, DRAM address counter AC add by 1.

When I/D = "0", cursor moves left, DRAM address counter AC subtract by 1.

S: Display shift

S	I/D	DESCRIPTION
H	H	Entire display shift left by 1
H	L	Entire display shift right by 1

- **DISPLAY STATUS**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
code	0	0	0	0	0	0	0	1	D	C	B

Controls display, cursor and blink ON/OFF.

D : Display ON/OFF control bit

When D = "1", display ON

When D = "0",display OFF , the content of DDRAM is not changed

C : Cursor ON/OFF control bit

When C = "1", cursor ON.

When C = "0", cursor OFF.

B : Blink ON/OFF control bit

When B = "1", cursor position blink ON. Then display data in cursor position will blink.

When B = "0", cursor position blink OFF

- **CURSOR AND DISPLAY SHIFT CONTROL**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
code	0	0	0	0	0	0	1	S/C	R/L	X	X

Instruction to move the cursor or shift the entire display. The content of DDRAM is not changed.

S/C	R/L	Description	AC Value
L	L	Cursor moves left by 1	AC=AC-1
L	H	Cursor moves right by 1	AC=AC+1
H	L	Display shift left by 1, cursor also follows to shift.	AC=AC
H	H	Display shift right by 1, cursor also follows to shift.	AC=AC

- **FUNCTION SET**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
code	0	0	0	0	0	0	1	DL	X	RE	X	X

DL : 4/8 BIT interface control bit

When DL = "1", **8 BIT** MPU bus interface

When DL = "0", **4 BIT** MPU bus interface

RE : extended instruction set control bit

When RE = "1", extended instruction set

When RE = "0", basic instruction set

In same instruction cannot alter DL and RE at once. Make sure that change DL first then RE.

- **SET CGRAM ADDRESS**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
code	0	0	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Set CGRAM address to address counter AC

AC range is 00H..3FH

Make sure that in extended instruction SR=0 (scroll address or RAM address select)

- **SET DDRAM ADDRESS**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
code	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Set DDRAM address to address counter (AC) .

First line AC range is 80H..8FH

Second line AC range is 90H..9FH

Third line AC range is A0H..AFH

Fourth line AC range is B0H..BFH

Please note that only 2 lines can be display at a time.

- **READ BUSY FLAG (BF) AND ADDRESS**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
code	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Read busy flag BF can check whether internal operation is finished. At the same time the value of address counter (AC) is also read. When BF = "1" new instruction will not be accepted. Must wait for BF = "0" for new instruction.

- **WRITE DATA TO RAM**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
code	1	0	D7	D6	D5	D4	D3	D2	D1	D0

Write data to internal RAM and alter the (AC) by 1

Each RAM address (CGRAM,DDRAM,IRAM…..) must write 2 consecutive bytes for 16 bit data. After the second byte the address counter will add or subtract by 1 according to the entry mode set control bit.

- **READ RAM DATA**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
code	1	1	D7	D6	D5	D4	D3	D2	D1	D0

Read data from internal RAM and alter the (AC) by 1

After address set to read (CGRAM,DDRAM,IRAM…..)a DUMMY READ is required.

There is no need to DUMMY READ for the following bytes unless a new address set instruction is issued.

Description of extended instruction set

- **STAND BY**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
code	0	0	0	0	0	0	0	0	0	1

Instruction to enter stand by mode. Any other instruction follows this instruction can terminate stand by.

The content of DDRAM remain the same.

- **VERTICAL SCROLL OR RAM ADDRESS SELECT**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
code	0	0	0	0	0	0	0	0	1	SR

When SR = "1", the vertical scroll address set is enabled.

When SR = "0", the IRAM address set **(extended instruction)** and CGRAM address set **(basic instruction)** is enabled.

- **REVERSE**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
code	0	0	0	0	0	0	0	0	1	R1	R0

Select 1 out of 4 lines to reverse the display and to toggle the reverse condition by repeating this instruction.

R1,R0 initial vale is 00. When set the first time the display is reversed and set the second time the display become normal.

R1	R0	Description
L	L	First line normal or reverse
L	H	Second line normal or reverse
H	L	Third line normal or reverse
H	H	Fourth line normal or reverse

Please note that only 2 lines out of 4 line display data can be displayed.

- **SLEEP**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
code	0	0	0	0	0	0	0	0	1	SL	0	0

SL=1: leave sleep mode

SL=0: enter sleep mode

- **EXTENED FUNCTION SET**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
code	0	0	0	0	0	0	1	DL	X	RE	G	X

DL : 4/8 BIT interface control bit

When DL = "1", **8 BIT** MPU interface

When DL = "0", **4 BIT** MPU interface

RE : extended instruction set control bit

When RE = "1", extended instruction set

When RE = "0", basic instruction set

G : Graphic display control bit

When G = "1", graphic display ON

When G = "0", Graphic display OFF

In same instruction cannot alter DL, RE and G at once. Make sure that change DL or G first and then RE.

- **SET IRAM OR SCROLL ADDRESS**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
code	0	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

SR=1:

AC5~AC0 is vertical scroll displacement address
SR=0: AC3~AC0 is ICON RAM address

- **SET GRAPHIC RAM ADDRESS**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
code	0	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Set GDRAM address to address counter AC .

First set vertical address and then horizontal address(write 2 consecutive bytes to complete vertical and horizontal address set)

Vertical address range is AC6...AC0

Horizontal address range is AC3…AC0

The address counter AC of graphic RAM (GRAM) only increment after write for horizontal address. After horizontal address=0FH it will automatically back to 00H. However, the vertical address will not increase as the result of the same action.

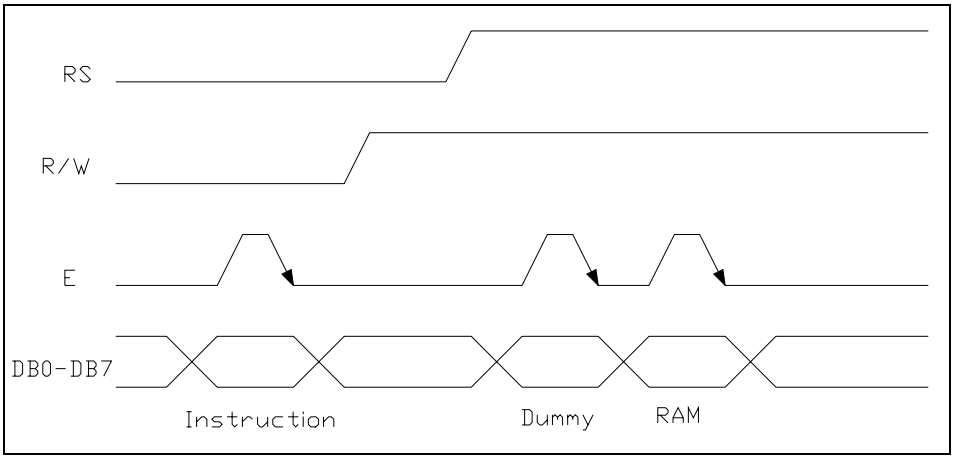
11. Parallel interface

ST7920 is in parallel mode by pulling up PSB pin. And can select 8 bit or 4-bit bus interface by function set instruction DL control bit. MPU can control (RS , RW , E , and DB0..DB7) pins to complete the data transmission.

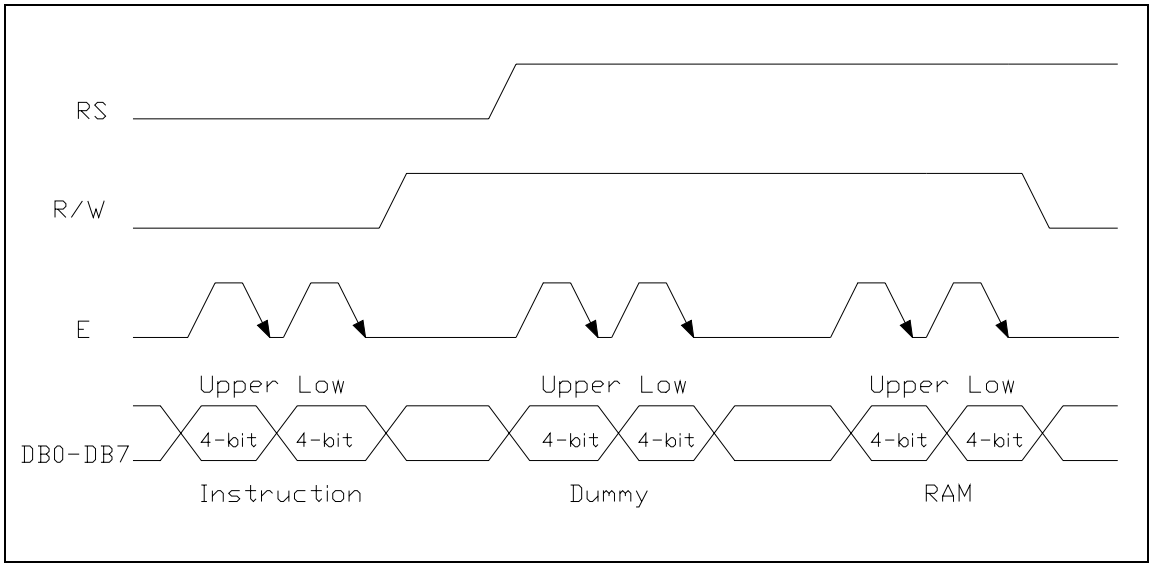
In 4-bit transfer mode, every 8 bits data or instruction is separated into 2 parts. Higher 4 bits

DB7~DB4 data will transfer.

First and placed into data pins (DB7~DB4). Lower 4 bits (DB3~DB0) data will transfer second and placed into data pins (DB7~DB4). (DB3~DB0) data pins are not used.



Timing Diagram of 8-bit Parallel Bus Mode Data Transfer



Timing Diagram of 4-bit Parallel Bus Mode Data Transfer

Serial interface :

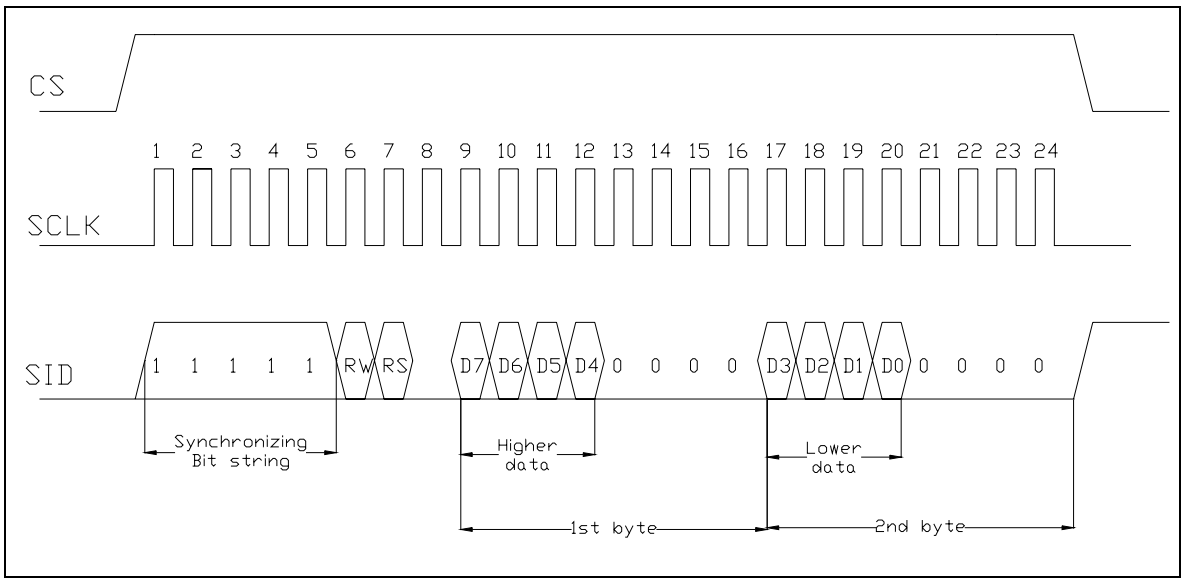
ST7920 is in serial interface mode when pull down PSB pin. Two pins (SCLK and SID) are used to complete the data transfer. Only write data is available.

When connecting several ST7920, chip select (CS) must be used. Only when (CS) is high the serial clock (SCLK) can be accepted. On the other hand, when chip select (CS) is low ST7920 serial counter and data will be reset. Transmission will be terminated and data will be cleared. Serial transfer counter is set to the first bit. For a minimal system with only one ST7920 and one MPU,
only SCLK and SID pins are necessary. CS pin should pull to high.

ST7920's serial clock SCLK is asynchronous to the internal clock and is generated by MPU. When multiple instruction/data is transferred instruction execution time must be considered. Must wait for the previous instruction to finish before sending the next. ST7920 has no internal instruction buffer area.

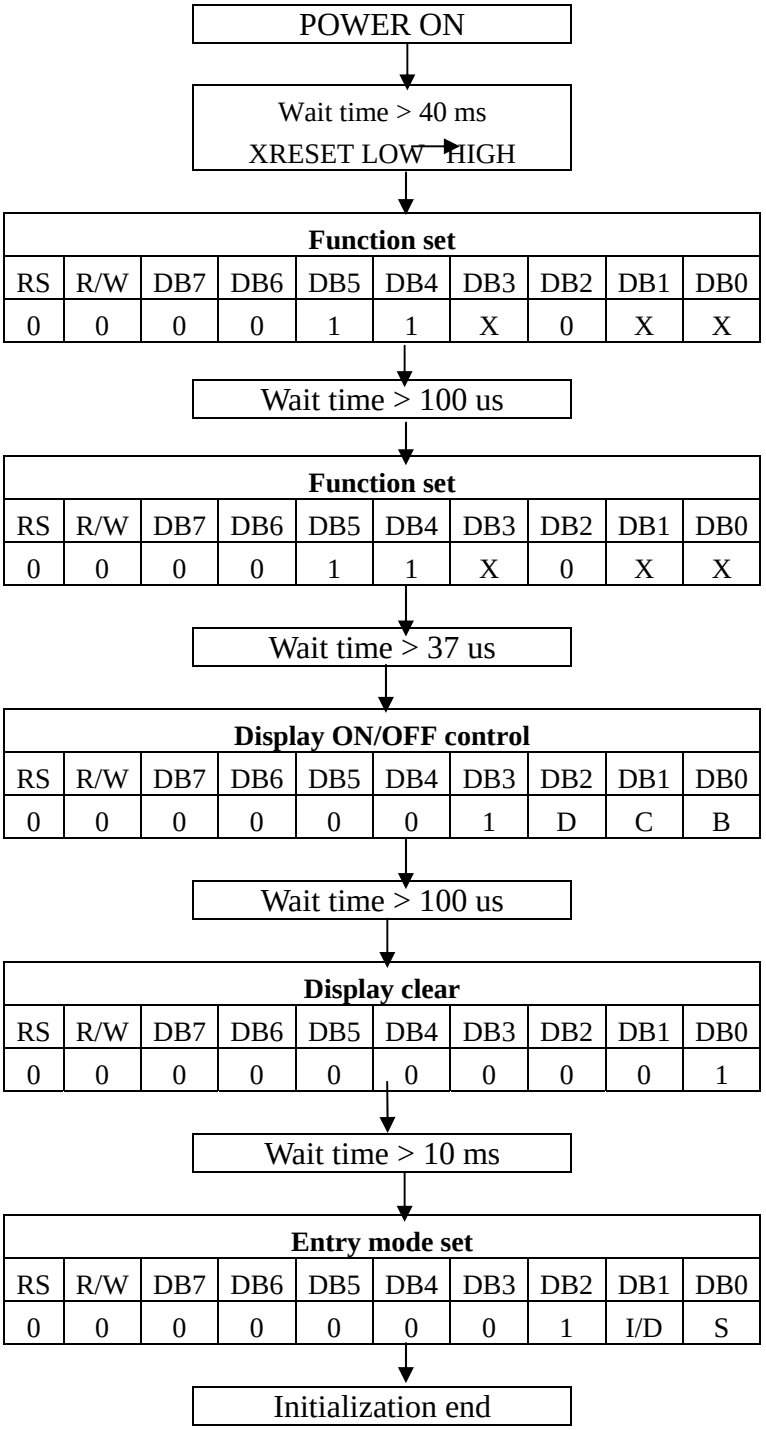
When starting a transmission a start byte is required. It consists of 5 consecutive "1"(sync character). Serial transfer counter will be reset and synchronized. Following 2 bits for read/write (RW) and register/data select (RS). Last 4 bits is filled by "0"

After receiving the sync character and RW and RS bits, every 8 bits instruction/data will be separated into 2 groups. Higher 4 bits (DB7~DB4) will be placed in first section followed by 4 "0". And lower 4 bits DB3~DB0 will be placed in second section followed by 4 "0".

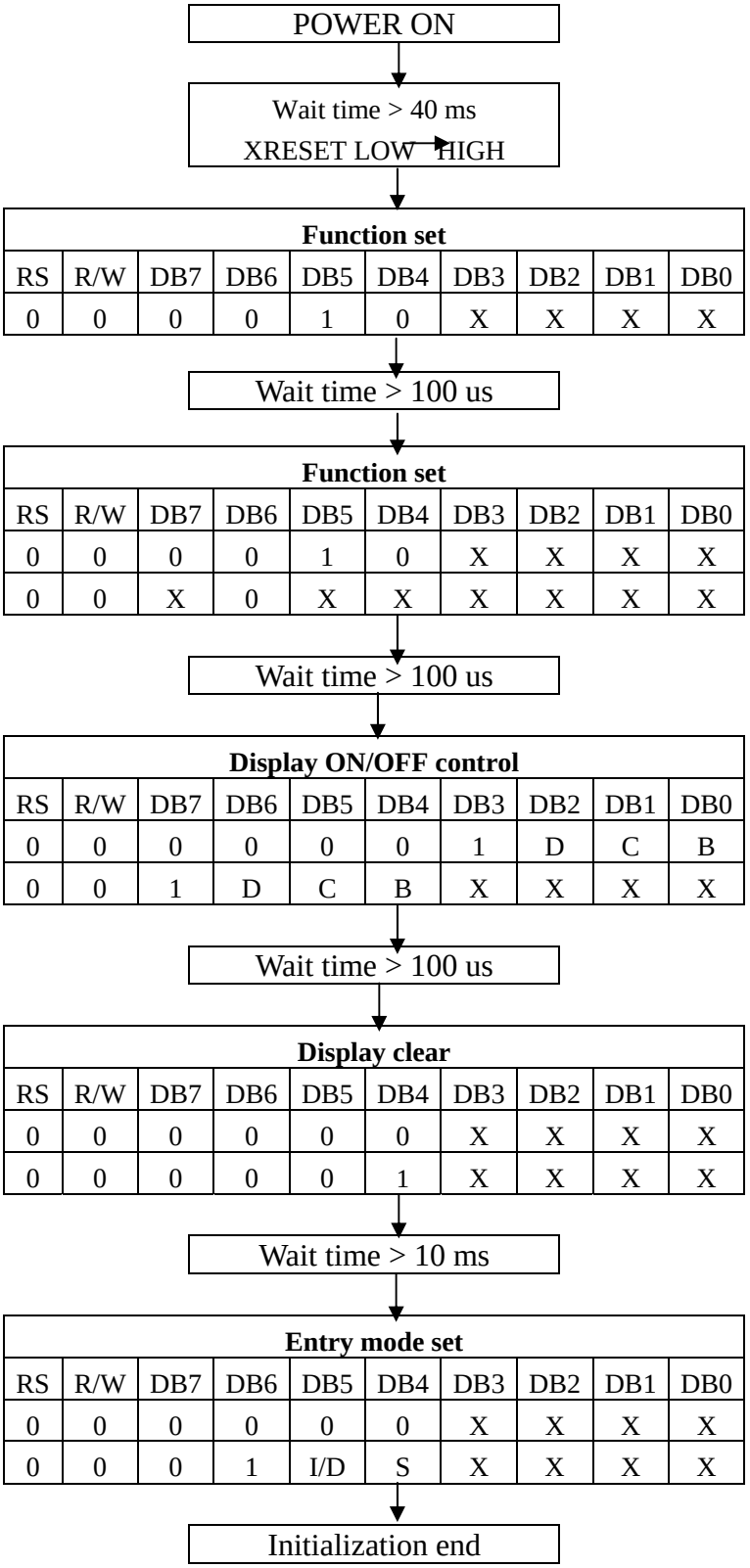


Timing Diagram of Serial Mode Data Transfer

8 bit interface：

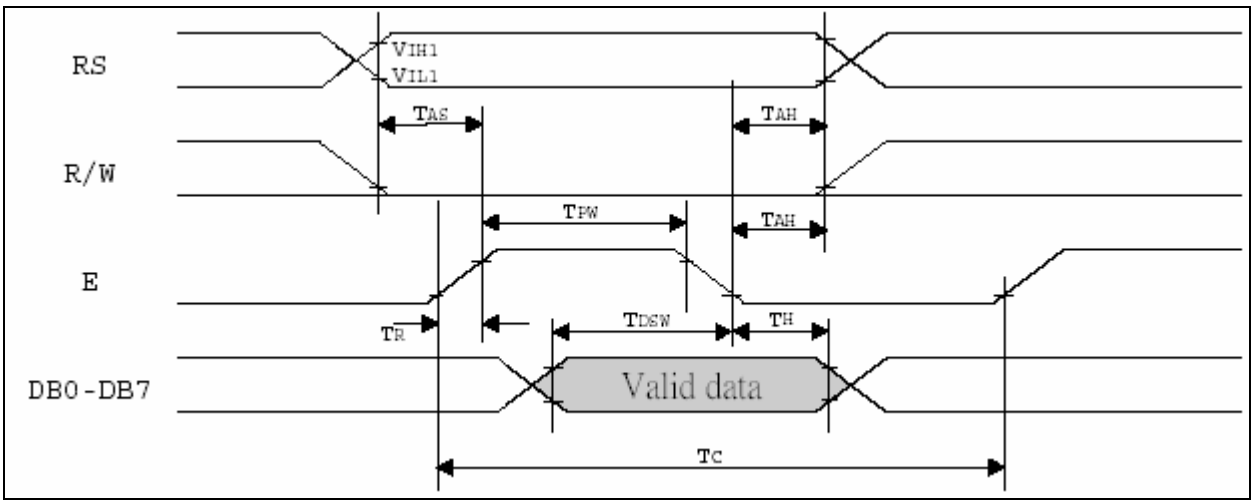


4 bit interface：

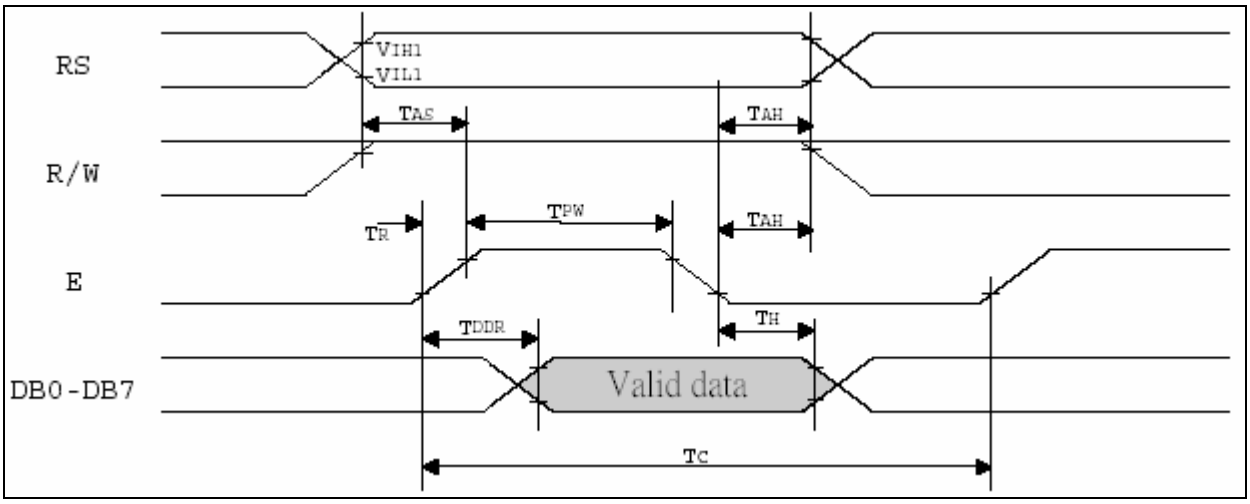


8 bit interface timing diagram

- MPU write data to ST7920

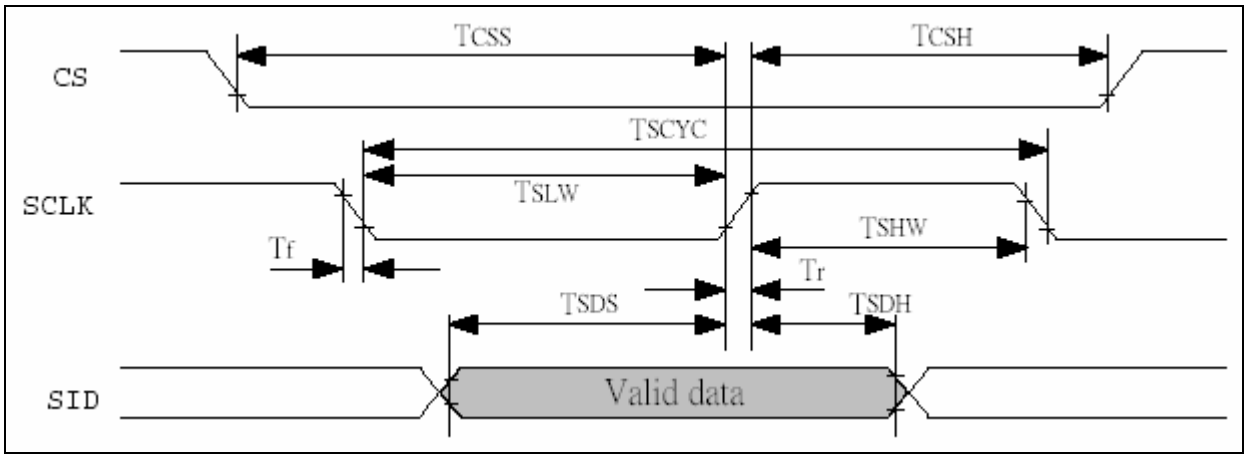


- **MPU read data from ST7920**



Serial interface timing diagram

- **MPU write data to ST7920**



Absolute Maximum Ratings

Characteristics	Symbol	Value
Power Supply Voltage	V_{DD}	-0.3V to +5.5V
LCD Driver Voltage	V_{LCD}	-0.3V to +7.0V
Input Voltage	V_{IN}	-0.3V to V_{DD}+0.3V
Operating Temperature	T_A	-20°C to +85°C
Storage Temperature	T_{STO}	-55°C to +125°C

DC Characteristics (T_A=25°C, V_{DD}=2.7V – 4.5V)

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage	–	2.7	–	5.5	V
V_{LCD}	LCD Voltage	V0 – Vss	3.0	–	5.5	V
Icc	Power Supply Current	f_{OSC} = 530KHz, V_{DD} = 3.0V Rf = 18 kΩ	–	0.20	0.45	mA
V_{IH1}	Input High Voltage (Except OSC1)	–	0.7 V_{DD}	–	V_{DD}	V
V_{IL1}	Input Low Voltage (Except OSC1)	–	-0.3	–	0.6	V
V_{IH2}	Input High Voltage (OSC1)	–	V_{DD}-1	–	V_{DD}	V
V_{IL2}	Input Low Voltage (OSC1)	–	–	–	1.0	V
V_{OH1}	Output High Voltage (DB0 – DB7)	I_{OH} = -0.1 mA	0.8V_{DD}	–	V_{DD}	V
V_{OL1}	Output Low Voltage (DB0 – DB7)	I_{OL} = 0.1 mA	–	–	0.1	V
V_{OH2}	Output High Voltage (Except DB0 – DB7)	I_{OH} = -0.04 mA	0.8 V_{DD}	–	V_{DD}	V
V_{OL2}	Output Low Voltage (Except DB0 – DB7)	I_{OL} = 0.04 mA	–	–	0.1 V_{DD}	V
I_{LEAK}	Input Leakage Current	V_{IN} = 0V TO V_{DD}	-1	–	1	µa
I_{PUP}	Pull Up MOS Current	V_{DD} = 3V	22	27	32	µ A

DC Characteristics (T_A = 25°C, V_{DD} = 4.5 V – 5 V)

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage	–	4.5	–	5.5	V
V_{LCD}	LCD Voltage	V0 – Vss	3.0	–	5.5	V
Icc	Power Supply Current	f_{OSC} = 540KHz, V_{DD} = 5 V Rf = 33kΩ	–	0.45	0.75	mA
V_{IH1}	Input High Voltage (Except OSC1)	–	0.7 V_{DD}	–	V_{DD}	V
V_{IL1}	Input Low Voltage (Except OSC1)	–	-0.3	–	0.6	V
V_{IH2}	Input High Voltage (OSC1)	–	V_{DD}-1	–	V_{DD}	V
V_{IL2}	Input Low Voltage (OSC1)	–	–	–	1.0	V
V_{OH1}	Output High Voltage (DB0 – DB7)	I_{OH} = -0.1 mA	0.8V_{DD}	–	V_{DD}	V
V_{OL1}	Output Low Voltage (DB0 – DB7)	I_{OL} = 0.1 mA	–	–	0.4	V
V_{OH2}	Output High Voltage (Except DB0 – DB7)	I_{OH} = -0.04 mA	0.8 V_{DD}	–	V_{DD}	V
V_{OL2}	Output Low Voltage (Except DB0 – DB7)	I_{OL} = 0.04 mA	–	–	0.1 V_{DD}	V
I_{LEAK}	Input Leakage Current	V_{IN} = 0V TO V_{DD}	-1	–	1	µA
I_{PUP}	Pull Up MOS Current	V_{DD} = 5 V	75	80	85	µ A

AC Characteristics (T_A = 25°C, V_{DD} = 4.5V) Parallel Mode Interface

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
Internal Clock Operation						
f_{OSC}	LCD Voltage	V0 – Vss	3.0	–	7	V
f_{EX}	Power Supply Current	f_{OSC} = 540KHz, V_{DD} = 5 V Rf = 33kΩ	–	0.45	0.75	mA
V_{IH1}	Input High Voltage (Except OSC1)	–	0.7 V_{DD}	–	V_{DD}	V
V_{IL1}	Input Low Voltage (Except OSC1)	–	-0.3	–	0.6	V
V_{IH2}	Input High Voltage (OSC1)	–	V_{DD}-1	–	V_{DD}	V
V_{IL2}	Input Low Voltage (OSC1)	–	–	–	1.0	V
V_{OH1}	Output High Voltage (DB0 – DB7)	I_{OH} = -0.1 mA	0.8V_{DD}	–	V_{DD}	V
V_{OL1}	Output Low Voltage (DB0 – DB7)	I_{OL} = 0.1 mA	–	–	0.4	V
V_{OH2}	Output High Voltage (Except DB0 – DB7)	I_{OH} = -0.04 mA	0.8 V_{DD}	–	V_{DD}	V
V_{OL2}	Output Low Voltage (Except DB0 – DB7)	I_{OL} = 0.04 mA	–	–	0.1 V_{DD}	V
I_{LEAK}	Input Leakage Current	V_{IN} = 0V TO V_{DD}	-1	–	1	µA
I_{PUP}	Pull Up MOS Current	V_{DD} = 5 V	75	80	85	µ A

AC Characteristics (T_A = 25°C, V_{DD} = 4.5V) Parallel Mode Interface

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
Internal Clock Operation						
f_{OSC}	OSC Frequency	R=33kΩ	480	540	600	KHz
External Clock Operation						
f_{EX}	External Frequency	–	480	540	600	KHz
	Duty Cycle	–	45	50	55	%
T_R,T_F	Rise/Fall Time	–	–	–	0.2	μ S
Write Mode (Writing data from MPU to ST7920)						
Tc	Enable Cycle Time	Pin E	1200	–	–	nS
T_{PW}	Enable Pulse Width	Pin E	140	–	–	nS
T_R,T_F	Enable Rise/Fall Time	Pin E	–	–	25	nS
T_{AS}	Address Setup Time	Pins : RS,RW,E	10	–	–	nS`
T_{AH}	Address Hold Time	Pins : RS,RW,E	20	–	–	nS
T_{DSW}	Data Setup Time	Pins : DB0-DB7	40	–	–	nS
T_H	Data Hold Time	Pins : DB0-DB7	20			nS
Read Mode (Reading Data from ST7920 to MPU)						
Tc	Enable Cycle Time	Pin : E	1200	–	–	nS
T_{PW}	Enable Pulse Width	Pin : E	140	–	–	nS
T_R,T_F	Enable Rise/Fall Time	Pin : E	–	–	25	nS
T_{AS}	Address Setup Time	Pins : RS,RW,E	10	–	–	nS
T_{AH}	Address Hold Time	Pins : RS,RW,E	20	–	–	nS
T_{DDR}	Data Delay Time	Pins : DB0-DB7	–	–	100	nS
T_H	Data Hold Time	Pins : DB0-DB7	20	–	–	nS
Interface Mode with LCD Driver (ST7921)						
T_{CWH}	Clock Pulse with High	Pins : CL1, CL2	800	–	–	nS
T_{CWL}	Clock Pulse With Low	Pins : CL1, CL2	800	–	–	nS
T_{CST}	Clock Setup time	Pins : CL1, CL2	500	–	–	nS
T_{SU}	Data Setup Time	Pin : D	300	–	–	nS
T_{DM}	Data Hold Time	Pin : D	300	–	–	nS
T_{PW}	Enable Pulse Width	Pin : M	-1000	–	1000	nS

AC Characteristics (T_A = 25°C, V_{DD} = 2.7V) Parallel Mode Interface

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
Internal Clock Operation						
f_{OSC}	OSC Frequency	R=18kΩ	470	530	590	KHz
External Clock Operation						
f_{EX}	External Frequency	–	470	530	590	KHz
	Duty Cycle	–	45	50	55	%
T_R,T_F	Rise/Fall Time	–	–	–	0.2	μ S
Write Mode (Writing data from MPU to ST7920)						
Tc	Enable Cycle Time	Pin E	1800	–	–	nS
T_{PW}	Enable Pulse Width	Pin E	160	–	–	nS
T_R,T_F	Enable Rise/Fall Time	Pin E	–	–	25	nS
T_{AS}	Address Setup Time	Pins : RS,RW,E	10	–	–	nS`
T_{AH}	Address Hold Time	Pins : RS,RW,E	20	–	–	nS
T_{DSW}	Data Setup Time	Pins : DB0-DB7	40	–	–	nS
T_H	Data Hold Time	Pins : DB0-DB7	20			nS
Read Mode (Reading Data from ST7920 to MPU)						
Tc	Enable Cycle Time	Pin : E	1800	–	–	nS
T_{PW}	Enable Pulse Width	Pin : E	320	–	–	nS
T_R,T_F	Enable Rise/Fall Time	Pin : E	–	–	25	nS
T_{AS}	Address Setup Time	Pins : RS,RW,E	10	–	–	nS
T_{AH}	Address Hold Time	Pins : RS,RW,E	20	–	–	nS
T_{DDR}	Data Delay Time	Pins : DB0-DB7	–	–	260	nS
T_H	Data Hold Time	Pins : DB0-DB7	20	–	–	nS
Interface Mode with LCD Driver (ST7921)						
T_{CWH}	Clock Pulse with High	Pins : CL1, CL2	800	–	–	nS
T_{CWL}	Clock Pulse With Low	Pins : CL1, CL2	800	–	–	nS
T_{CST}	Clock Setup time	Pins : CL1, CL2	500	–	–	nS
T_{SU}	Data Setup Time	Pin : D	300	–	–	nS
T_{DM}	Data Hold Time	Pin : D	300	–	–	nS
T_{PW}	Enable Pulse Width	Pin : M	-1000	–	1000	nS

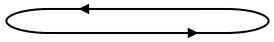
12. Quality Assurance

Screen Cosmetic Criteria

No.	Defect	Judgment Criterion	Partition
1	Spots	A) Clear Size: d mm — Acceptable Qty in active area d ≦ 0.1 — Disregard 0.1<d≦ 0.2 — 6 0.2<d≦ 0.3 — 2 0.3<d — 0 Note: Including pin holes and defective dots which must be within one pixel size. B) Unclear Size: d mm — Acceptable Qty in active area d ≦ 0.2 — Disregard 0.2<d≦ 0.5 — 6 0.5<d≦ 0.7 — 2 0.7<d — 0	Minor
2	Bubbles in Polarize	Size: d mm — Acceptable Qty in active area d≦ 0.3 — Disregard 0.3<d≦ 1.0 — 3 1.0<d≦ 1.5 — 1 1.5<d — 0	Minor
3	Scratch	In accordance with spots cosmetic criteria. When the light reflects on the panel surface, the scratches are not to be remarkable.	Minor
4	Allowable Density	Above defects should be separated more than 30mm each other.	Minor
5	Coloration	Not to be noticeable coloration in the viewing area of the LCD panels. Back-light type should be judged with back-light on state only.	Minor

13. Reliability

Content of Reliability Test

Environmental Test			
Test Item	Content of Test	Test Condition	Applicable Standard
High Temperature storage	Endurance test applying the high storage temperature for a long time.	80℃ 200hrs	——
Low Temperature storage	Endurance test applying the high storage temperature for a long time.	-30℃ 200hrs	——
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	70℃ 200hrs	——
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-20℃ 200hrs	——
High Temperature/ Humidity Storage	Endurance test applying the high temperature and high humidity storage for a long time.	80℃,90%RH 96hrs	——
High Temperature/ Humidity Operation	Endurance test applying the electric stress (Voltage & Current) and temperature / humidity stress to the element for a long time.	70℃,90%RH 96hrs	——
Temperature Cycle	Endurance test applying the low and high temperature cycle. -30℃ 25℃ 80℃  30min 5min 30min 1 cycle	-30℃/80℃ 10 cycles	——
Mechanical Test			
Vibration test	Endurance test applying the vibration during transportation and using.	10~22Hz→ 1.5mmp-p 22~500Hz→ 1.5G Total 0.5hrs	——
Shock test	Constructional and mechanical endurance test applying the shock during transportation.	50G Half sign wave 11 msedc 3 times of each direction	——
Atmospheric pressure test	Endurance test applying the atmospheric pressure during transportation by air.	115mbar 40hrs	——
Others			
Static electricity test	Endurance test applying the electric stress to the terminal.	VS=800V,RS=1.5kΩ CS=100pF 1 time	——

***Supply voltage for logic system=5V. Supply voltage for LCD system =Operating voltage at 25℃

14. Backlight Information

Specification

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITION
Supply Current	ILED	–	40	60	mA	V=3.5V
Supply Voltage	V	-	3.5	3.9	V	-
Reverse Voltage	VR	-	-	5	V	-
Luminous Intensity	IV	-	20	-	cd/m^2	ILED=40mA
Wave Length	λ p	–		–	nm	ILED=40mA
Life Time	-	-	**50K**	-	Hr.	V≦ 3.5V
Color	Green					